

## TITLE

### ESD PROTECTION CIRCUIT WITH VERY LOW INPUT CAPACITANCE FOR HIGH-FREQUENCY I/O PORTS

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## BACKGROUND OF THE INVENTION

### Field of the Invention

10 The present invention relates to an electrostatic discharge (ESD) protection circuit with low capacitance, in particular, to an ESD protection circuit suitable for high-frequency I/O ports.

### Description of the Related Art

15 As the manufacturing process for integrated circuit (IC) improves, the gate oxide layer of metal-oxide-semiconductor transistors (MOS) becomes thinner and more easily damaged by unexpected stress. Thus, it has become more and more important to provide effective ESD protection circuit in I/O ports or between power supply lines to prevent internal elements from being damaged by ESD stress.

20 Fig. 1(a) is a conventional ESD protection circuit composed of two diodes, being put between an input/output (I/O) pad 10 and an internal circuit 12. P-type diode  $D_{p1}$  is connected between VDD and I/O pad 10, n-type diode  $D_{n1}$  is connected between VSS and I/O pad 10. Fig. 1(b) is an improved version of Fig. 1(a), being a two-stage ESD protection circuit. Primary ESD protection circuit 14 is composed of  $D_{p1}$  and  $D_{n1}$ , while secondary ESD protection 16 is composed of  $D_{p2}$  and  $D_{n2}$ . In general, the

p-type diode in Fig. 1(a) or Fig. 1(b) has a PN junction formed by placing a p-type heavily doped area 20 in an n-type well 24, as shown in Fig. 2. The n-type diode in Fig. 1(a) or Fig. 1(b), in general, has a PN junction formed by placing a heavily doped n-type area 28 in a p-type well 22, as shown in Fig. 3. The N-type well 24 and the p-type well 22 are usually directly in contact with the p-type substrate 26.

There are four different pin combinations to verify the ESD level of an input (or output) pin of an IC, as the PS-, NS-, PD- and ND-modes ESD stresses shown in Fig. 4. They are:

- (i) PS-mode ESD stress: a positive ESD pulse is applied to a tested IC pin with the VSS pin relatively grounded, while other non-tested pins are all floating;
- (ii) NS-mode ESD stress: a negative ESD pulse is applied to a tested IC pin with the VSS pin relatively grounded, while other non-tested pins are floating;
- (iii) PD-mode ESD stress: a positive ESD pulse is applied to a tested IC pin with the VDD pin relatively grounded, while other non-tested pins are floating; and
- (iv) ND-mode ESD stress: a negative ESD pulse is applied to a tested IC pin with the VDD pin relatively grounded, while other non-tested pins are flowing.

The I/O pad 10 of Fig. 1(a) and Fig. 1(b) under these four different ESD-stress modes has a different ESD sustained voltage level. The ESD level of a pin is defined as the lowest voltage (in magnitude) that the pin can sustain. In PD mode (or NS mode), the  $D_{p1}$  (or  $D_{n1}$ ) is forward-biased to release ESD current. The forward bias voltage of the diode is about 0.8 V in the general CMOS manufacturing process. In PS (or ND) mode,  $D_{n1}$  (or  $D_{p1}$ ) is reverse-biased to break down, releasing ESD current. During

breakdown, the voltage across of the diode is about 10 V in a 0.35  $\mu\text{m}$  CMOS manufacturing process. The generated power of the diode is  $I_{\text{diode}} * V_{\text{diode}}$ , in which  $I_{\text{diode}}$  is the current flowing through the diode and  $V_{\text{diode}}$  is the voltage across the diode. From above, the generated power of the diode during breakdown will be much larger than the generated power during forward bias. Therefore, the design of the  $D_{p1}$  and  $D_{n1}$  emphasizes how to make  $D_{p1}$  and  $D_{n1}$  release ESD current effectively during ND- and PS-mode ESD stress without burning themselves out.

In order to reach the commercial requirement of  $\pm 2000$  V for human body model (HBM) in the commercial specification,  $D_{p1}$  and  $D_{n1}$  are generally designed as large-sized elements. The device width may be as large as several hundred micrometers. Large elements have a large volume to efficiently dissipate the heat generated during the release of ESD stress, thus preventing burnout of  $D_{p1}$  and  $D_{n1}$  during ESD events.

However, large elements will cause large loading to the I/O port. Fig. 5 is the equivalent circuit of Fig. 1(a), showing parasitic capacitors therein. In view of small signal circuit analysis, the input equivalent capacitance  $C_{\text{input}}$  seen from I/O pad 10 of Fig. 1(a) is approximately equal to  $C_{\text{pad}} + C_{jp} + C_{jn}$ ; in which,  $C_{\text{pad}}$  is the parasitic capacitance formed by a large metal plate constituting a bonding pad and the surrounding conductor,  $C_{jp}$  is the parasitic capacitance of PN junction of  $D_{p1}$  (as shown in Fig. 2),  $C_{jn}$  is the parasitic capacitance of the PN junction of  $D_{n1}$  (as shown in Fig. 3). In general, a bonding pad with a  $100\mu\text{m} * 100\mu\text{m}$  metal plate has approximately 0.5pF parasitic capacitance. The parasitic capacitance of  $D_{p1}$  (or  $D_{n1}$ ) with an element width of few hundred micrometers is about 2~4pF. Roughly

speaking, the input equivalent capacitance  $C_{input}$  is about 5pF, where most of it is contributed by  $D_{pi}$  or  $D_{n1}$ . Such high input capacitance will lower the response speed of the I/O port at high frequencies. For high-frequency IC or high-speed IC, in particular, the smaller the loading of the I/O port the better. Thus, circuit designs as shown in Fig. 1(a) or Fig. 1(b) are not suitable for high-frequency or high-speed ICs.

In addition, for the I/O port with current as the input signal or high-frequency I/O port, an additional resistor, as R in Fig. 1(a) and Fig. 1(b), will cause non-linear frequency response and introduce thermal noise to distort the input signal. Such distortion is not allowed. Under this limit, conventional ESD protection circuits of Fig. 1(a) and Fig. 1(b) are not suitable for high-frequency IC application. Therefore, it is a challenge for ESD protection circuit designers to design an ESD protection circuit capable of high-speed IC and bearing high ESD stress.

#### SUMMARY OF THE INVENTION

The main object of the present invention is to provide an ESD protection circuit with high ESD tolerance level and small capacitance, especially suitable for high frequency IC I/O ports.

According to the above object, the present invention proposes an ESD protection circuit with low input capacitance loading, suitable for an I/O pad. The ESD protection circuit contains a plurality of diodes and a power-rail ESD clamp circuit. The diodes are stacked between a first power line and the I/O pad. The power-rail ESD clamp circuit is coupled between the first power line and a second power line. During normal power

operation, the diodes are reverse-biased and the power-rail ESD clamp circuit is turned off. When an ESD event occurs between the second power line and the I/O pad, the power-rail ESD clamp circuit is turned on to conduct ESD current through the forward-biased diodes.

Each diode has a PN junction formed between a first well of a second conductivity type and a doped region of a first conductivity type therein. A deep well of a first conductivity is located under the first well to isolate the first well from a substrate of the second conductivity.

Due to the stack structure, the equivalent capacitance of the stack diodes will be smaller than the parasitic capacitance of a single diode. Hence one advantage of the present invention is to effectively reduce a large amount of input capacitance loading.

Another advantage of the present invention is that the diodes are forward-biased to release ESD stress, unlike the prior art, which is reverse-biased to release ESD stress. Thus, each diode can be constructed as a smaller sized element. The chip area required by the I/O port can be reduced and, as a result, the input capacitance is further reduced.

The present invention also provides a power-rail ESD clamp circuit, suitable for an integrated circuit, coupled between two power lines. The ESD clamp circuit between power lines includes a substrate-triggered NMOS and an ESD detection circuit. The NMOS includes a gate, two source/drains and a substrate. The two source/drains are coupled to the two power lines respectively. When an ESD event is detected, the ESD detection circuit provides a bias current to the substrate of the NMOS,

and a bias voltage to the gate of the NMOS element, to trigger the NMOS and release ESD stress.

Because the gate and the base of the NMOS element are simultaneously biased during the ESD event, the triggering speed can be greatly increased. Thus, the ESD current between the power lines can be released rapidly to protect the internal circuit of the integrated circuit.

### BRIEF DESCRIPTION OF THE DRAWINGS

The present invention can be more fully understood by reading the subsequent detailed description in conjunction with the examples and references made to the accompanying drawings, wherein:

Fig. 1(a) shows a conventional ESD protection circuit consisted of two diodes;

Fig. 1(b) shows a two-stage ESD protection circuit in the prior art;

Fig. 2 illustrates the structural cross-sectional view of the conventional p-type diode;

Fig. 3 illustrates the structural cross-sectional view of the conventional n-type diode;

Fig. 4 introduces the four different ESD stress modes;

Fig. 5 is the circuit diagram in Fig. 1(a) with its parasitic capacitors;

Fig. 6 is an ESD protection circuit according to the present invention;

Figs. 7 to 10 illustrate ESD current paths in the ESD protection circuit under the four different ESD stress modes;

Fig. 11 is an n-type diode of the present invention and its representative symbols;

Fig. 12 is the structural cross-sectional view of the  $M_{ESD}$  element in Fig. 6 and the symbol schematic view;

Fig. 13 is the improved ESD protection circuit of Fig. 6 according to the invention;

5 Fig. 14 is an ESD protection circuit with three diodes stacked between a power line and a pad according to the present invention;

Fig 15 represents the HSPICE simulation result of the input equivalent capacitance of Fig. 5, Fig. 6 and Fig. 14;

10 Fig. 16 illustrates an NMOS with deep N well structure and the parasitic n-type diode therein applied in the present invention; Fig. 17 illustrates a PMOS and the parasitic p-type diode therein applied in the present invention; and

15 Figs. 18 to 25 are 8 embodiments utilizing the diodes with NMOS or PMOS structures according to the present invention.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

In order to reduce the input equivalent capacitance, the present invention proposes a stack structure of diodes as ESD protection circuit, as shown in Fig. 6. Two n-type diodes ( $D_{n1}$  and  $D_{n2}$ ) stack between a pad 30 and a power line VSSA. Two p-type diodes ( $D_{p1}$  and  $D_{p2}$ ) stack between the pad 30 and VDDA. During the normal operation of an integrated circuit,  $D_{p1}$ ,  $D_{p2}$ ,  $D_{n1}$ ,  $D_{n2}$  are reverse-biased but not breakdown, such that electrical signals at the pad 30 can be transmitted to the internal circuit 32. The values of the parasitic capacitance of the diodes are represented by  $C_{jn1}$ ,  $C_{jn2}$ ,  $C_{jp1}$  and  $C_{jp2}$ , as shown in Fig. 6. Because of the stack structure, the equivalent capacitance input can be effectively reduced. For example, set  $C_{jn1}=C_{jn2}=C_{jn}$  and  $C_{jp1}=C_{jp2}=C_{jp}$ , the input equivalent capacitance  $C_{input}$  becomes

20  
25  
30

$$C_{input} = C_{pad} + (C_{jn} + C_{jp}) / 2$$

In comparison to the conventional ESD protection circuit in Fig. 5, the capacitance (or loading) generated by ESD protection circuit of Fig. 6 is only halved. Thus, the frequency response of the input port can be effectively improved.

However, the breakdown voltage of the stacked diodes will be two times the breakdown voltage of a single diode. The higher breakdown voltage means that the internal circuit 32 is easier to be damaged in an ESD event (for example, ND or PS modes). In order to assure the ESD robustness of the I/O port, there is a VDDA-to-VSSA ESD clamp circuit 34 coupled between VDDA and VSSA, as shown in Fig. 6. VDDA-to-VSSA ESD clamp circuit 34 consists of a RC delay circuit 36 formed by resistor R1 and capacitance C1 in series, an inverter 38 formed by  $M_{p1}$  and  $M_{n1}$ , and a substrate-triggered NMOS  $M_{ESD}$ . RC delay circuit 34 is used to detect occurrence of the ESD event, inverter 38 provides a bias current to trigger npn bipolar junction transistor parasitizing in  $M_{ESD}$ , thereby releasing ESD current. The gate of  $M_{ESD}$  is coupled to VSSA through resistor R2 to assure  $M_{ESD}$  is turned off during non-ESD event.

Figs. 7 to 10 show the ESD protection circuits of the present invention together with the corresponding ESD current paths during the four ESD stress modes. Fig. 7 illustrates the ESD current path under PS mode. ESD current  $I_{ESD}$  from pad 30, through forward-biased  $D_{p1}$  and  $D_{p2}$ , conducts into VDDA. Then, VDDA-to-VSSA ESD clamp circuit 34 is turned on so that  $I_{ESD}$  flows to VSSA from VDDA, and flows out of IC from grounded VSSA. Fig. 8 illustrates the ESD current path under NS mode ESD stress.  $I_{ESD}$ , through forward-biased  $D_{n1}$  and  $D_{n2}$ , flows from VSSA into pad 30. Fig. 9 shows the condition under PD mode,  $I_{ESD}$  flows from pad 30,



through forward-biased  $D_{p1}$  and  $D_{p2}$ , into VDDA. Fig. 10 shows the condition under ND mode, ESD clamping circuit 34 between power lines is triggered to conduct current because of the ESD stress so that  $I_{ESD}$  flows from VDDA to VSSA, then through forward-biased  $D_{n1}$  and  $D_{n2}$ ,  $I_{ESD}$  flows from VSSA into pad 30.

From the above analysis, in an ESD event, stacked diodes always conduct ESD current under forward-bias conditions. The power generated for the diode under forward-bias is smaller than that for the diode during breakdown. Thus, in comparison to the conventional ESD protection circuit utilizing only a single diode between a pad and a power line, the ESD robustness of the ESD protection circuit of the present invention can be greatly increased.

However, the conventional n-type diode in Fig. 3 has a common p-type substrate 26. Thus, such an n-type diode cannot be stacked in series, to meet the connection requirement for  $D_{n1}$  and  $D_{n2}$  as shown in Fig. 6.

In order to achieve the configuration of the stacked diode circuit in Fig. 6, the present invention proposes a novel n-type diode structure, as shown in Fig. 11. Fig. 11 shows the novel n-type diode structure and its symbols used later in this specification. The n-type diode structure used in the present invention contains an N+ doped region 40 in a p-type well 42. N+ doped region 40 is the cathode of the n-type diode. P-type well 42 and the P+ doped region 48 thereon is the anode of the n-type diode. The entire n-type diode is surrounded by an n-type well 50 and the deep n-type well 44, so that p-type well 42 and p-type substrate 46 are separated from each other. The n-type well 50 and the deep n-type well 44 are coupled to VDDA through N+ doped region 52. Deep n-type well structures are commonly

used in radio frequency IC or dynamic random access memory (DRAM) IC, and usually separate a common p-type substrate from p-type wells in which NMOS is placed, preventing noise from migrating through the common p-type substrate. The stacked diode circuit in Fig. 6 can be realized using the n-type diode in the isolated p-type well.

The substrate-triggered NMOS  $M_{ESD}$  in Fig. 6 can also use a deep n-type well to isolate the p-type well and the common p-type substrate 46. Fig. 12 is the cross-sectional view of the  $M_{ESD}$  in Fig. 6 and its symbol schematic view. The n-type well 56 and the deep n-type well 54 separate the p-type well 58 from the common p-type substrate 46.  $M_{ESD}$  forms in the isolated p-type well 58. The source and drain of the  $M_{ESD}$  are N+ doped regions 62 and 60 respectively, its substrate (node) is p-type well 58, as a contact point through P+ doped area 64. In this way, the output terminal of the inverter 38 in Fig. 6 can control the turning on and off of parasitic npn transistor (formed by the N+ doped region 60, the p-type well 58 and the N+ doped region 62) by biasing the p-type well 58. Because the isolation of the deep n-type well, the triggered current from the inverter 38 will not be branched to p-type substrate 46 and efficiently drive  $M_{ESD}$ , such that the turn-on rate of  $M_{ESD}$  can be increased.

Fig. 13 is an improved ESD protection circuit of Fig. 6. In order to increase the turn-on rate of the VDDA-to-VSSA ESD clamp circuit 34, a bias voltage can be applied to the gate of  $M_{ESD}$ . In Fig. 13, inverter 38 not only provides the bias current into the substrate of the  $M_{ESD}$ , but also provides the bias voltage on the gate of  $M_{ESD}$ . In order to prevent the bias voltage on the gate from being overlarge, possibly damaging  $M_{ESD}$ , a plurality of diodes  $D_{R1} \dots D_{R4}$  are stacked between the MESD gate and VSSA.

$D_{R1}...D_{R4}$  clamp the largest voltage at the  $M_{ESD}$  gate. When an ESD event occurs, inverter 38 provides current to the base of the parasitic npn bipolar junction transistor, and at the same time pulls up the  $M_{ESD}$  gate to the clamp voltage limited by  $D_{R1}...D_{R4}$ . The number of diodes stacked between the  $M_{ESD}$  gate and VSSA can be different depending upon the different applications, and is not limited to four. Another way to prevent the voltage at the gate from getting too large is to place a Zener diode (not shown) coupled between the gate and VSSA, to replace the stacked plurality of the diodes  $D_{R1}...D_{R4}$ . When an ESD event occurs, the Zener diode is reverse-biased to enter breakdown condition, the fixed breakdown voltage of the Zener diode limits the amplitude of the bias voltage at the gate, thereby  $M_{ESD}$  being protected.

Once the turn-on rate of VDDA-to-VSSA ESD detection circuit 34 is sped up, the number of the diodes stacked between the power line (VDDA or VSSA) and the pad 30 can be further increased to obtain a smaller input equivalent capacitance. Fig. 14 is an ESD protection circuit diagram with three diodes stacked between power lines and the pad according to the present invention. Three n-type diodes ( $D_{n1}$ ,  $D_{n2}$ , and  $D_{n3}$ ) stacked between the pad 30 and VSSA; three p-type diodes ( $D_{p1}$ ,  $D_{p2}$ , and  $D_{p3}$ ) stacked between the pad 30 and VDDA. If every N type diode has the same parasitic capacitance  $C_{jn}$ , and every p-type diode has the same parasitic capacitance  $C_{jp}$ , the input equivalent capacitance in Fig. 14 is

$$C_{input} = C_{pad} + (C_{jp} + C_{jn})/3$$

Hence, when the number of the stacked diodes increases, input equivalent capacitance lowers. Lower input equivalent capacitance is required by both the high speed IC and the high frequency IC.

The main spirit of the present invention is to lower the effective input capacitance by stacking diodes, and, by employing a VDDA-to-VSSA ESD clamp circuit, solve the high breakdown voltage problem induced by the stacked diodes.

Fig. 15 is the HSPICE simulation result of the input capacitance in Figs. 5, 6 and 14; wherein VDDA is 3V, VSSA is ground. Input equivalent capacitance in Fig. 16 is almost constant and does not change greatly as voltage of the junction pad varies. From Fig. 15, the input equivalent capacitance of the ESD protection circuit of a single diode (as shown in Fig. 5) is about 3pF. The input equivalent capacitance of the ESD protection circuit of two stacked diodes (as shown in Fig. 6) is about 1.5pF. The input equivalent capacitance of the ESD protection circuit of three stacked diodes (as shown in Fig. 14) is lowered to about 0.5pF. Hence, the effect of increasing the number of the stacked diodes to lower input equivalent capacitance can be seen.

The diodes of the present invention need only be stackable; they are not limited to the structure shown in Fig. 11. For example, some of the diodes that can be used include p-type diodes, n-type diodes, NMOS diodes, PMOS diodes, the n-type diodes that parasitize in the drain of NMOS, or the p-type diodes that parasitize in the drain of PMOS. NMOS (or PMOS) diode refers to an NMOS (or PMOS) whose gate and source are connected together as an anode (or cathode) and its drain is used as a cathode (or anode). The different diodes can be swapped with one another.

Fig. 16 is a schematic of the n-type diode that parasitizes around a drain of an NMOS and can be used in the present invention. The drain of the NMOS in Fig. 16 is N+ doped region 64. The bulk of the NMOS is a p-type well 66, which is separated

from other p-type wells (not shown) by an n-type well 68 and a deep n-type well 70. The PN junction between the drain and the bulk is also an n-type diode, which can be employed in the present invention. The gate of NMOS can be coupled to the power line VSSA in the circuit so that NMOS is turned-off during normal operation; or is coupled to its own source, to form an additional NMOS diode. Both can be used in the present invention.

Fig. 17 is a schematic of the p-type diode that parasitizes around a drain of a PMOS and can be used in the present invention. The drain of the PMOS is a P+ doped region 72. The bulk of the PMOS is an n-type well 74. The n-type well 74 and other n-type wells (not shown) are separated by the p-type substrate 46. The PN junction between the drain and the bulk of the PMOS is also a p-type diode. The gate of the PMOS can be coupled to the highest voltage VDDA in the circuit so that PMOS is at turn-off state during normal operation; or is coupled to the source thereof to form an additional PMOS diode. Both can be used in the present invention.

Figs. 18 to 25 are ESD protection circuits utilizing the junction diodes between the drain and the bulk of the NMOS and PMOS according to the present invention. In Fig. 18, the connection of the  $MD_{p3}$  represents the parallel combination of two types of diodes. One is a PMOS diode (because the gate is coupled to the source), the other is p-type diode (because the bulk is coupled to the source), so the current conductivity can be greatly increased. In the same way, the connection of the  $MD_{n3}$  represents the parallel combination of two types of the diodes. One is an NMOS diode (because the gate is coupled to the source); the other is an n-type diode (because the bulk is coupled to the source).

Fig. 19 uses two PMOS ( $MD_{p2}$  and  $MD_{p3}$ ) and two NMOS ( $MD_{n2}$  and  $MD_{n3}$ ) as diodes. The gates of  $MD_{p2}$  and  $MD_{p3}$  are connected to VDDA. The gates of  $MD_{n2}$  and  $MD_{n3}$  are connected to VSSA.

The order of the stacked diode can be changed as wished. In Figs. 18 and 19, the NMOS and PMOS diodes are placed closest to the power lines (VDDA or VSSA). Fig. 20 and 21 are embodiments of two different orders, the gate of  $MD_{p1}$  wherein is connected to its own source, but can also be connected to VDDA. The gate of  $MD_{n1}$  is connected to its own source, but can also be connected to VSSA.

Fig. 22 and 23 are schematics of two ESD protection circuits formed by stacking three types of diodes, wherein the types of diodes stacked between VDDA and I/O pad can include a general n-type or p-type diode, a diode generated by NMOS and a diode generated by PMOS. The stacked diode circuit in the ESD protection circuit of the present invention can completely use diodes generated by PMOS or NMOS, as shown in Fig. 24 and 25.

In comparison to the prior art of ESD protection circuit, where a single diode is set between a pad and a power line, there is a plurality of diodes stacked between a power line and a pad in the present invention. The object of greatly reducing input equivalent capacitance is achieved. On the other hand, the ESD protection circuit between the power lines in the present invention solves the problem of lowered ESD robustness due to the stacked diodes. Hence, the ESD protection circuit of the present invention is particularly suitable in the I/O port of a high frequency or high speed IC.

While the invention has been described by way of examples and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments.

On the contrary, it is intended to cover various modifications and similar arrangements as would be apparent to those skilled in the art. Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.

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